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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,479	07/23/2003	Amit Ramchandran	021202-003720US	1300

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,479	RAMCHANDRAN, AMIT	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-5,7-11,13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki (patent No. 5,694,613) in view of Bartkowiak (patent No. 5,771,362).

2. Suzuki taught the invention substantially as claimed including a data processing ("DP") system comprising: (As per claims 1,7,13,15):

a) Computational unit in an adaptable computing engine wherein the computational unit includes a clock signal (e.g., see figs.7,13);

b) One or more functional unit (36) coupled to a bus (bus coupled to the registers in fig. 13 or the bus for transmitting the interrupts (INT) in figs. 1,13) wherein the one or more functional unit include functional unit input (input to arithmetic logic unit);

c) At least one register coupled between the bus and the input to the at least one functional unit input (pipeline register 34 in figure 1 or pipeline registers 106,34,32,102) (in figure 13 coupled between interrupt bus (INT) and arithmetic logic unit); and

d) A control signal for selectively causing the at least one register to hold the data value from the bus for one or more processing cycles (e.g. see the output of elements 10,104,30,28,100 in figs. 3,5 and 13 and col. 7, lines 26-50); and

e) (As per claims 13,15) data path from the input register to a given stage in the execution pipeline so that a value provided by the register is available for use at a time of execution of the given stage (e.g. see figs. 1,7, 13).

3. Suzuki did not expressly detail (claims 1,7,13,15), that the at least one functional unit in the one or more functional units, the data value being obtainable at the input at a start of a next processor cycle upon being needed. Bartkowiak however taught (e.g., see fig. 1 input registers 32a,32b,32c,32d,32e,32f directly connected to the bus and to input of the corresponding functional unit that store input data for the corresponding functional unit (20,22,24)(e.g., see col. 5, lines 9-50). Clearly in this configuration the input data value or operand stored in the input register for the corresponding functional unit would have been obtainable by the corresponding functional unit as needed at the input at a start of a next processor clock cycle upon being needed. Additionally Barkowiak taught that some operations required multiple clock cycles and with configuration of input register clearly this would have allow the system to store the input data multiple cycles at least when a preceding operation lasted multiple cycles and retrieve the data as needed. (e.g., see col. 5, lines 9-33).

4. As to the further limitations of claims 17-20 the configuration of the input registers provided at the input of the corresponding functional unit would have provided the input data without performing access or access command to memory. All that would have

been required to access the input data would have been a enable or clock signal to the input register (e.g., see col. 5, lines 9-33 and fig. 1 of Bartkowiak).

5. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Suzuki and Bartkowiak. Both references were directed to the problems of providing data and control for pipelined processing in a DP system (e.g., see col. 5, lines 9-33 and fig. 1 of Bartkowiak; and fig. 13 and col. 1, lines 16-45 of Suzuki). One of ordinary skill in the DP art would have motivated incorporate the Barkkowiak teachings of input registers located at the inputs of the functional units for storing operands at least to reduce timing constraint as to when the data is available from the bus as operands could be stored in the input register when the operands were available from the bus, and the functional could access the input when needed.

6. As per claim 2, Suzuki taught circuitry for selectively providing a constant value (selector and flip-flop)(e.g., see figs.3, 4, 5, 6 and col. 7, lines 26-50).

7. As per claim 3, Suzuki taught the computational unit coupling a pair of registers such that the pair of registers is responsive to a control signal value (one of registers 106 or 34 are paired with one of registers 32 or 102 using gates 114 and gates 116) (e.g., see fig. 13).

8. As per claim 4, Suzuki taught a computational unit comprising control circuitry (104,30,28,100) for setting the pair of registers to predetermined states based on the control signal values (e.g., see col. 7, lines 19-50).

9. As per claim 5, the claim requires one of the listed states to be provided by the system and the listed state of hold, hold or load, load and both are provided by the Suzuki system (e.g., see col. 7, lines 7-39 and fig. 13).

10. As to claim 7, Suzuki taught registers (32, 34, 106, 102) at inputs to functional units, wherein the registers are coupled to a bus for obtaining data from the bus (e.g., see fig. 13); and a control signal for selectively causing the registers to hold a data value from the bus for one or more processor cycles (the control signals output from selectors (28, 30, 100, 104) (e.g., see fig. 13 and col. 7, lines 19-50).

11. As per claim 8, Suzuki taught the register includes circuitry for selectively providing a constant value (e.g., see col. 7, lines 19-50).

12. As per claim 9, Suzuki taught the computational unit a coupling a pair of registers such that the pair of registers is responsive to a control signal value (one of registers 106 or 34 are paired with one of registers 32 or 102 using gates 114 and gates 116) (e.g., see fig. 13).

13. As per claim 10, Suzuki taught a computational unit comprising control circuitry (104,30,28,100) for setting the pair of registers to predetermined states based on the control signal values (e.g., see col. 7, lines 19-50).

14. As per claim 11, the claim requires one of the listed states to be provided by the system and the listed state of hold, hold or unload, unload and both are provided by the Suzuki system (e.g., see col. 7, lines 7-39 and fig. 13).

15. As per claims 14,16 Suzuki taught the register includes circuitry for selectively providing a constant value (e.g., see col. 7, lines 19-50).

16. Claims 6,12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki in view of Bartkowiak as applied to claims 1-5, and 7-11 above, and further in view of Edwards (patent No. 5,534,796).

17. Edwards taught (claims 6,12) control signals including unload, load and clear. Using these signals in the Suzuki system would have required six signals (three signals for two register and selectors and three signals for the other two registers and selectors). These six signals along with the hold signal of Suzuki would have provided seven control signals (e.g., see fig. 3 of Edwards and fig. 13 of Suzuki and col. 7, lines 7-39 of Suzuki).

18. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Edwards and Suzuki. Both references were directed to clocking of elements within a processor including the clocking of a pipeline register. One of ordinary skill in the art would have been motivated to add the Edwards teachings of load, unload and clear signals for pipeline registers to the Suzuki system at least because it would have provided more flexibility as to the number of cycles to hold data and provided the ability to selectively clear out old data from the register.

Response to Arguments

The change in scope of the amended claims has necessitated a new search.

Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

ERIC COLEMAN
PRIMARY EXAMINER